

Fig. 1

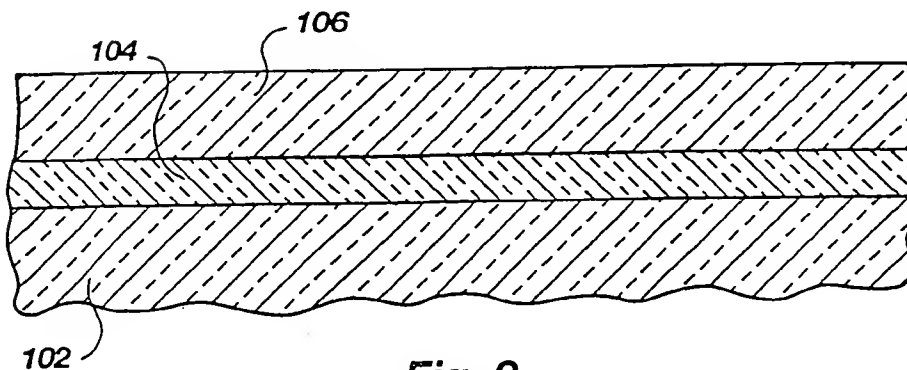


Fig. 2

TITLE: TECHNIQUE FOR ELIMINATION OF PITTING ON SILICON
SUBSTRATE DURING GATE STACK ETCH

Inventor: Pan et al.
Serial No.: 09/073,494
Docket No.: 2269-2915.1US

2/14

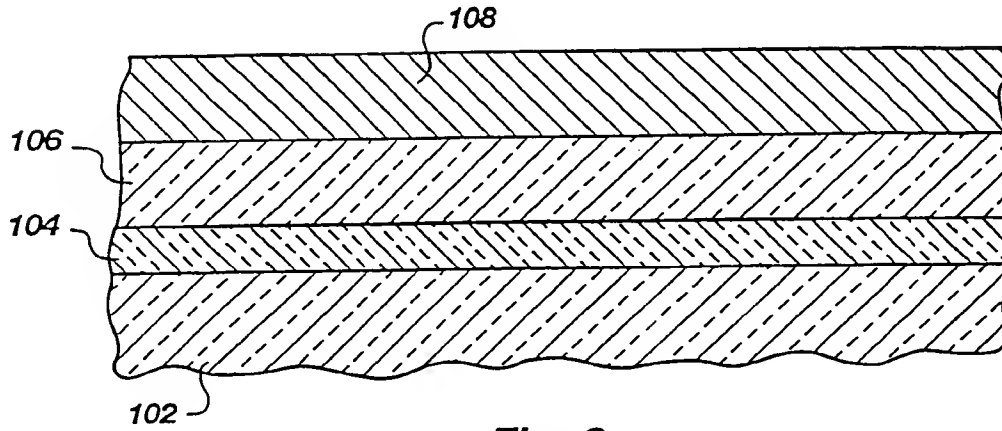
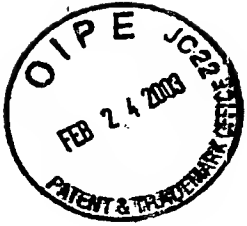


Fig. 3

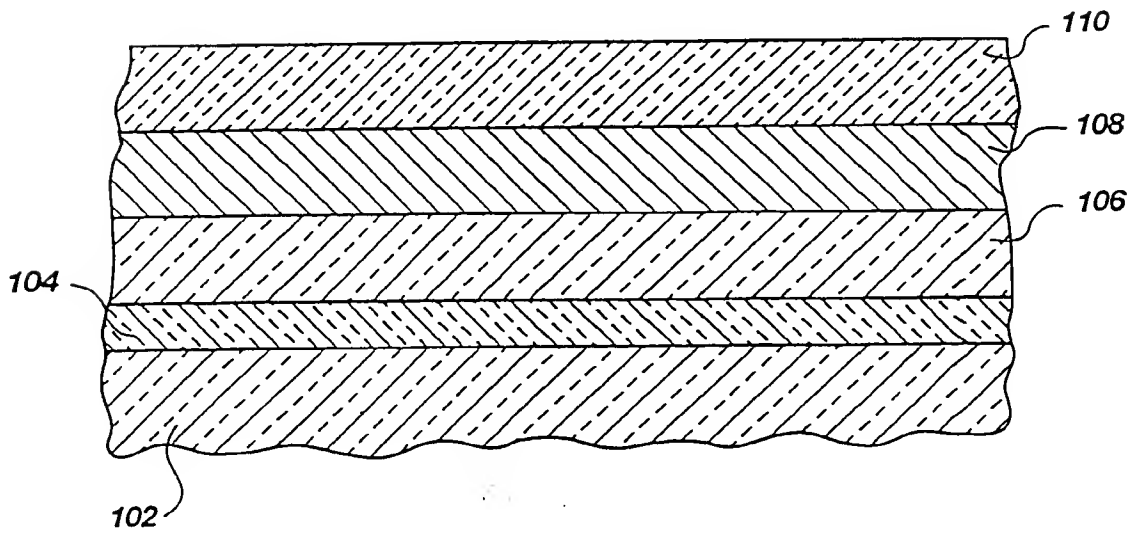


Fig. 4



3/14

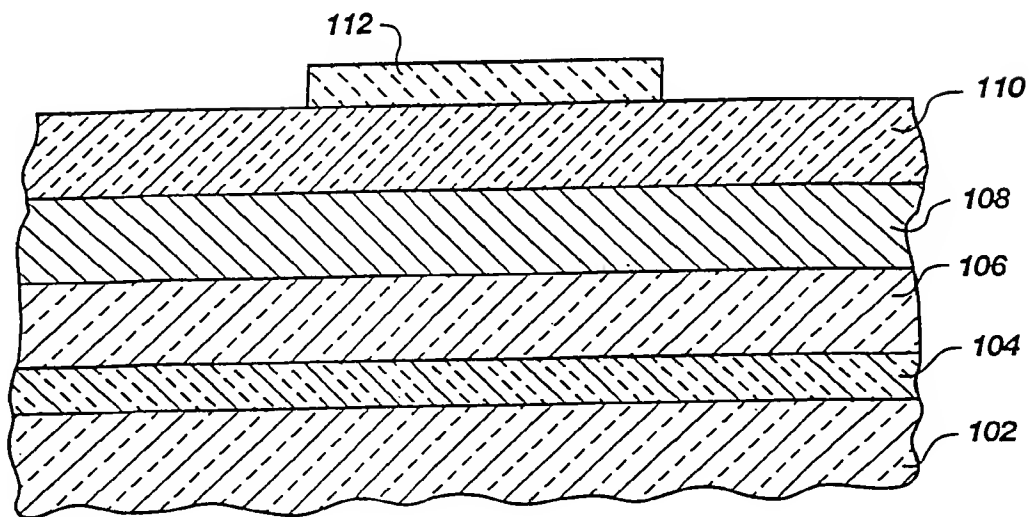


Fig. 5

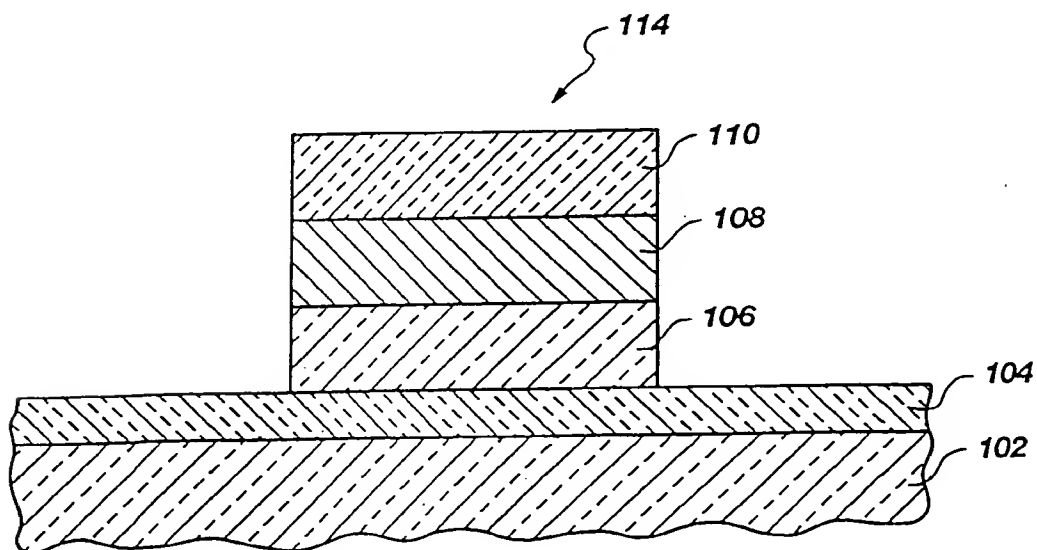


Fig. 6



4/14

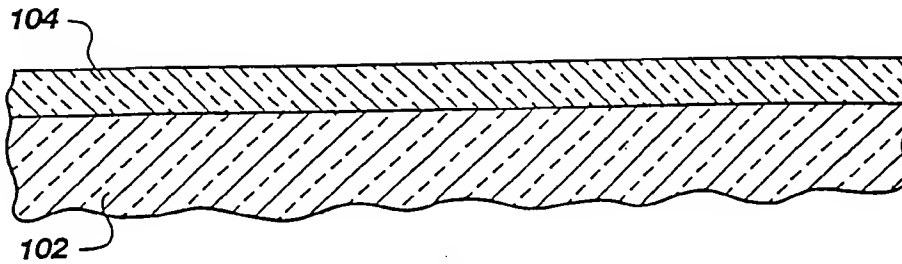


Fig. 7

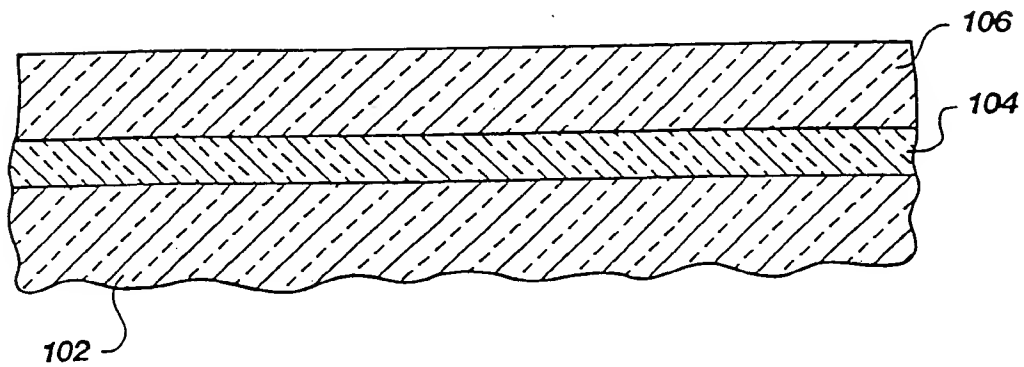


Fig. 8



TITLE: TECHNIQUE FOR ELIMINATION OF PITTING ON SILICON
SUBSTRATE DURING GATE STACK ETC

Inventor: Pan et al.
Serial No.: 09/073,494
Docket No.: 2269-2915.1US

5/14

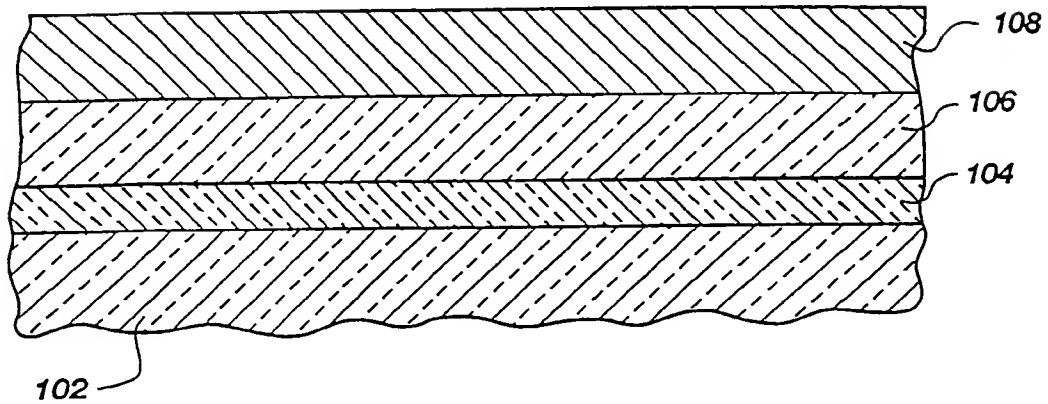


Fig. 9

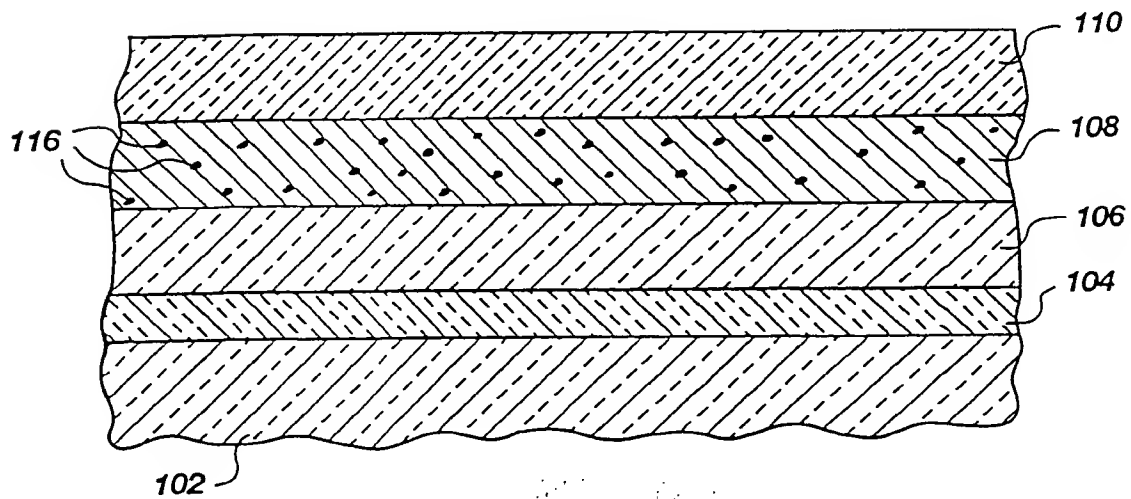


Fig. 10

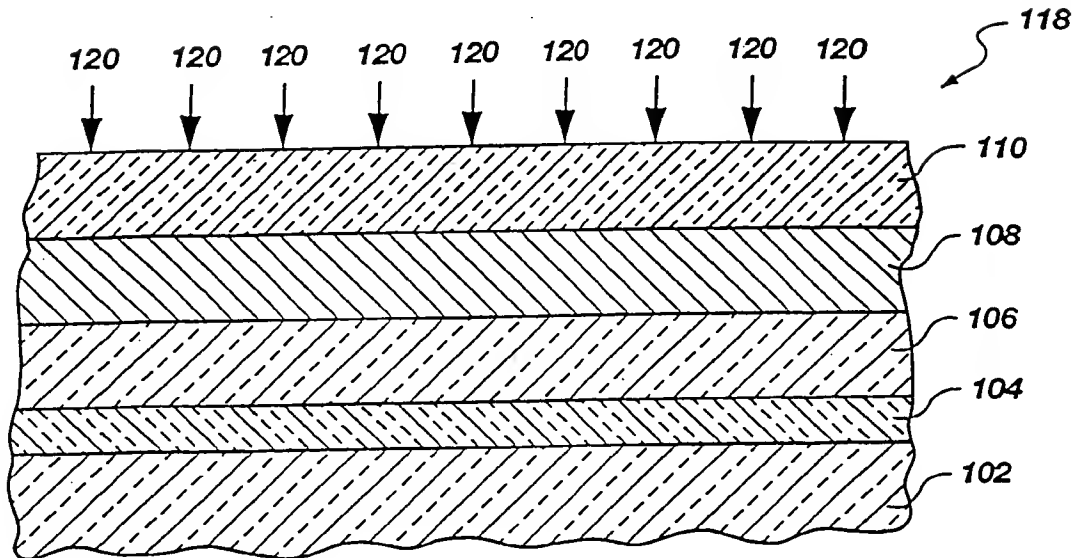


Fig. 11

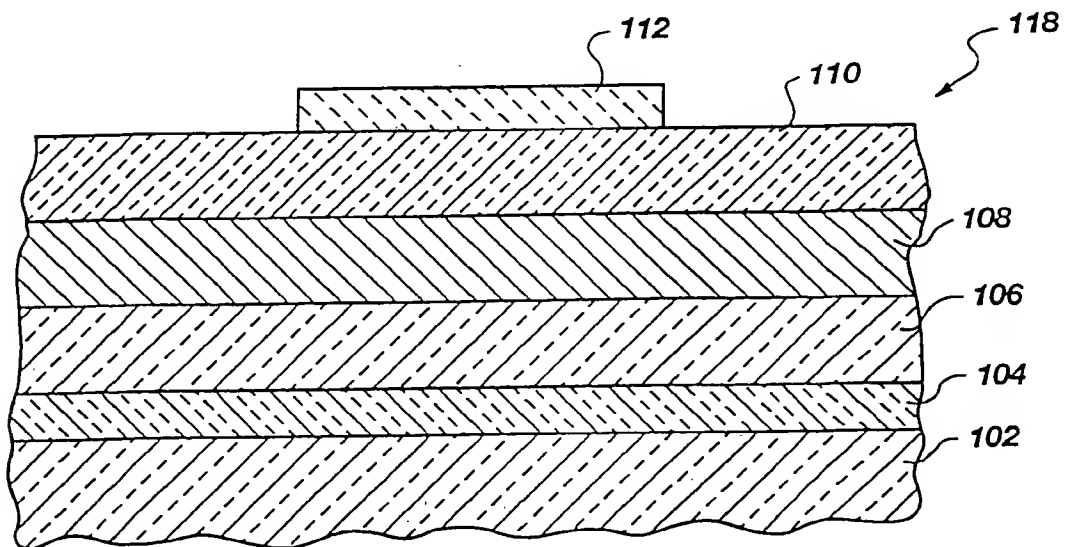


Fig. 12

TITLE: TECHNIQUE FOR ELIMINATION OF PITTING ON SILICON
SUBSTRATE DURING GATE STACK ETCH

Inventor: Pan et al.
Serial No.: 09/073,494
Docket No.: 2269-2915.1US

7/14

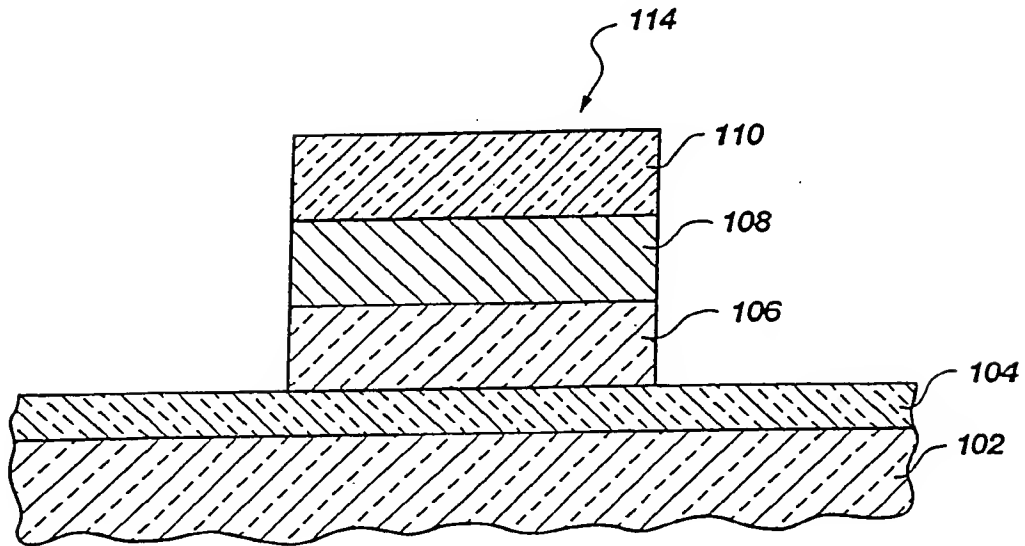


Fig. 13

8/14

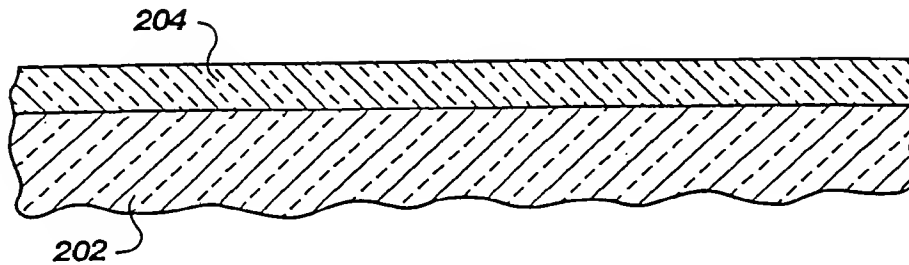


Fig. 14
(PRIOR ART)

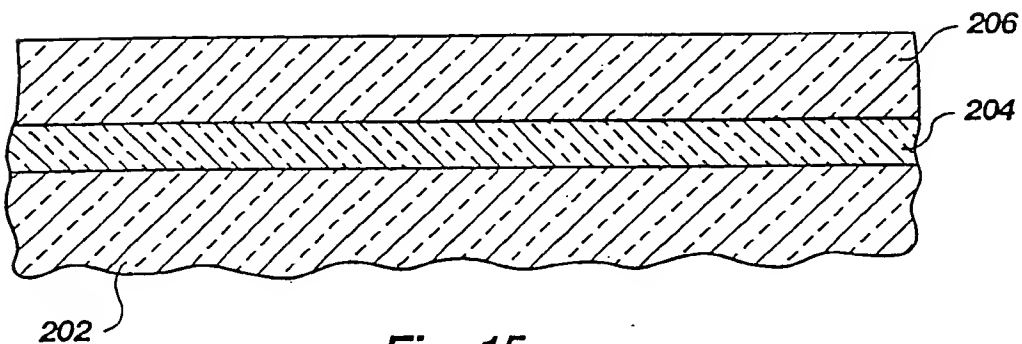


Fig. 15
(PRIOR ART)

9/14

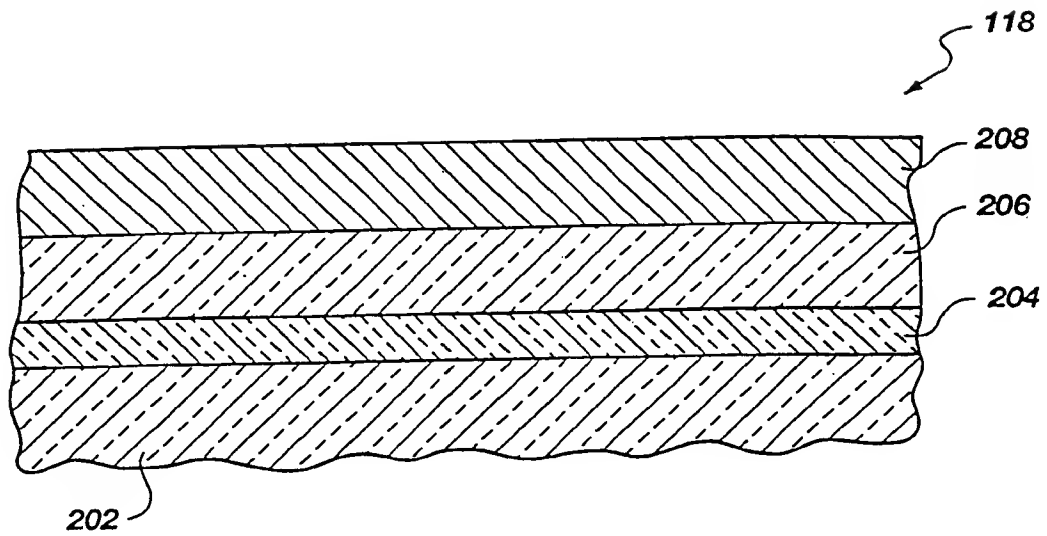


Fig. 16
(PRIOR ART)

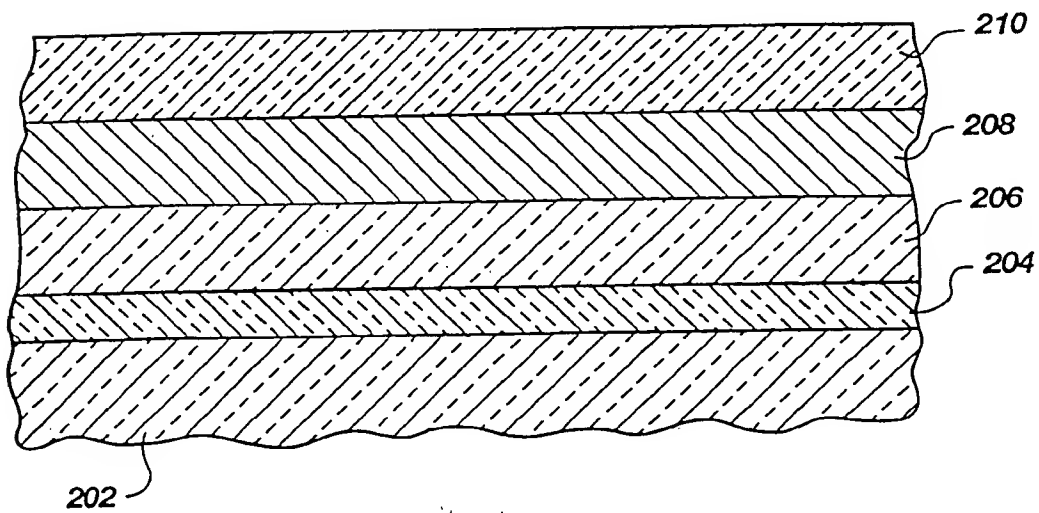


Fig. 17
(PRIOR ART)

10/14

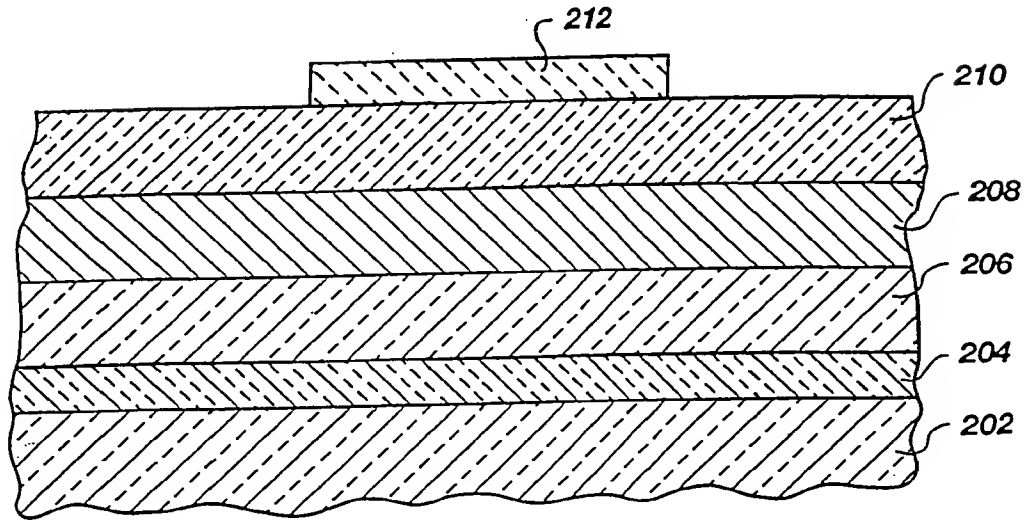


Fig. 18
(PRIOR ART)

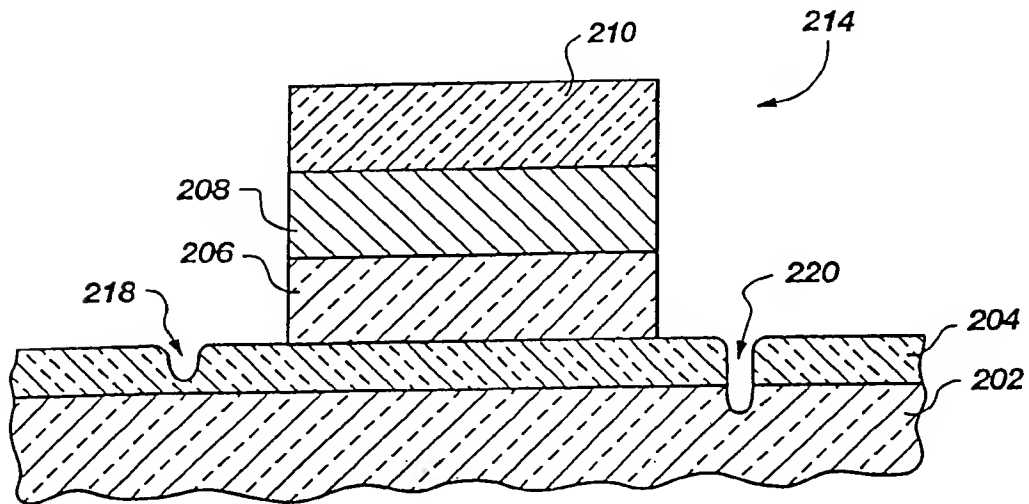


Fig. 19
(PRIOR ART)

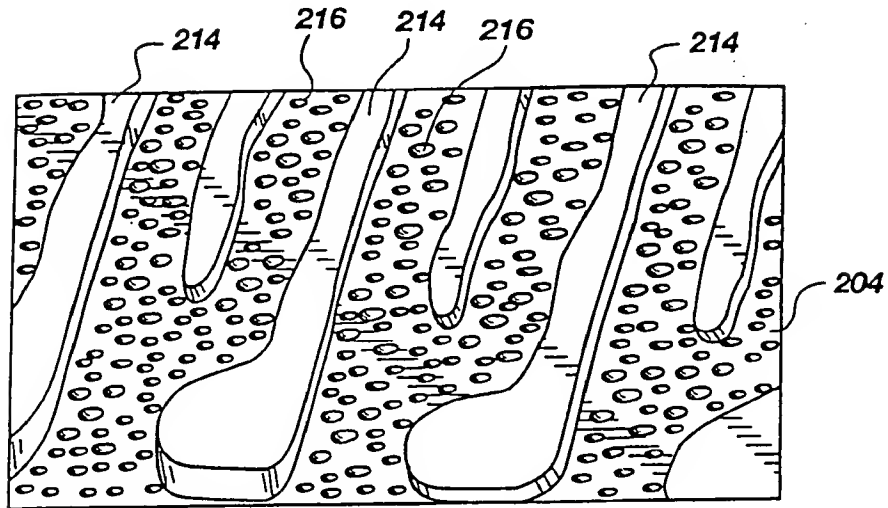


Fig. 20
(PRIOR ART)

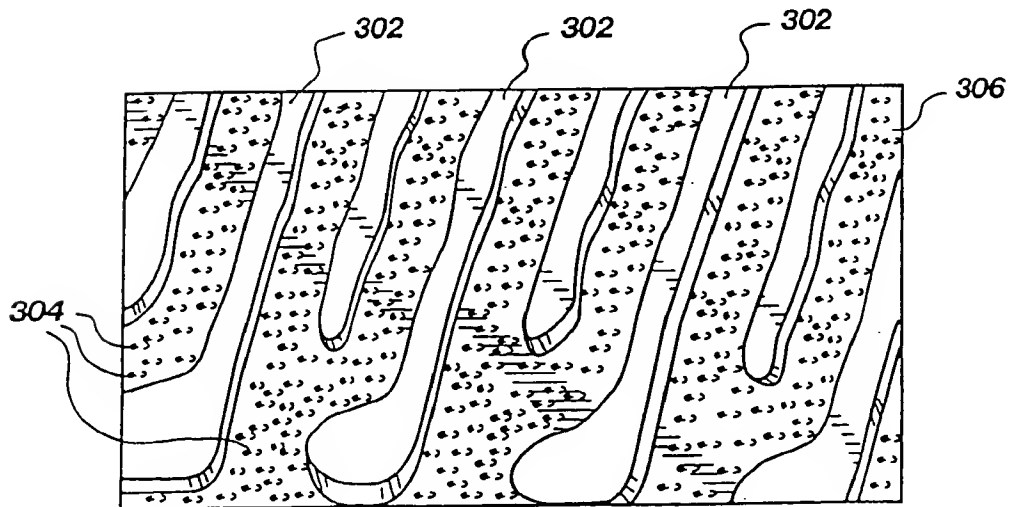


Fig. 21
(PRIOR ART)

TITLE: TECHNIQUE FOR ELIMINATION OF PITTING ON SILICON
SUBSTRATE DURING GATE STACK ETC

Inventor: Pan et al.
Serial No.: 09/073,494
Docket No.: 2269-2915.1US

12/14

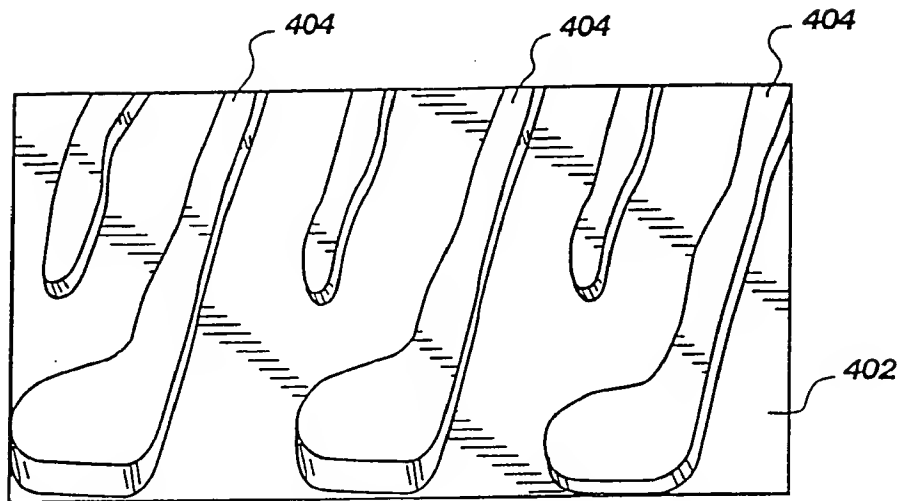


Fig. 22

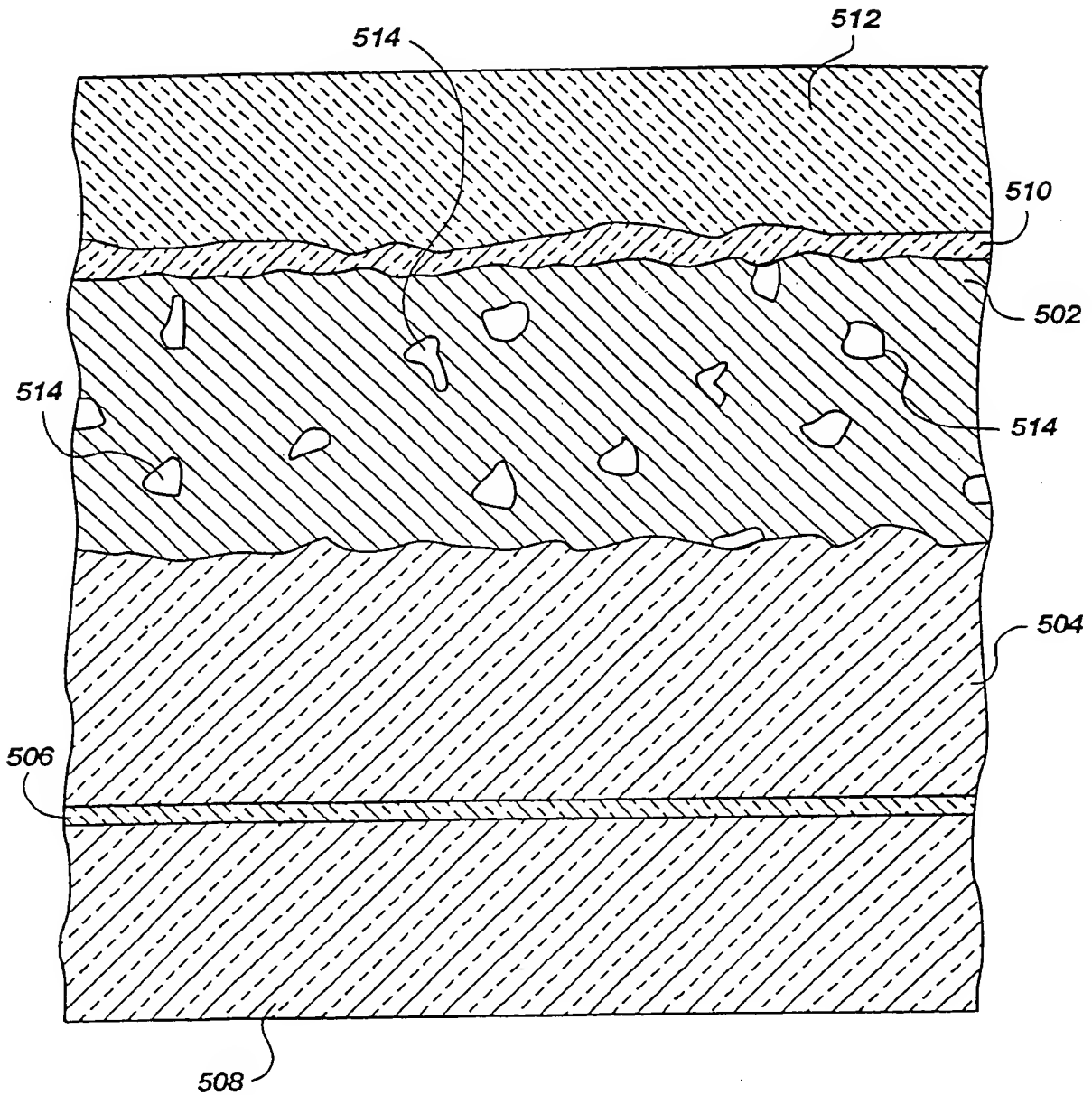
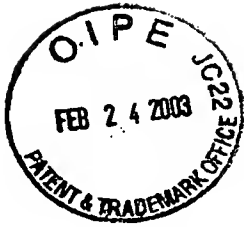


Fig. 23
(PRIOR ART)

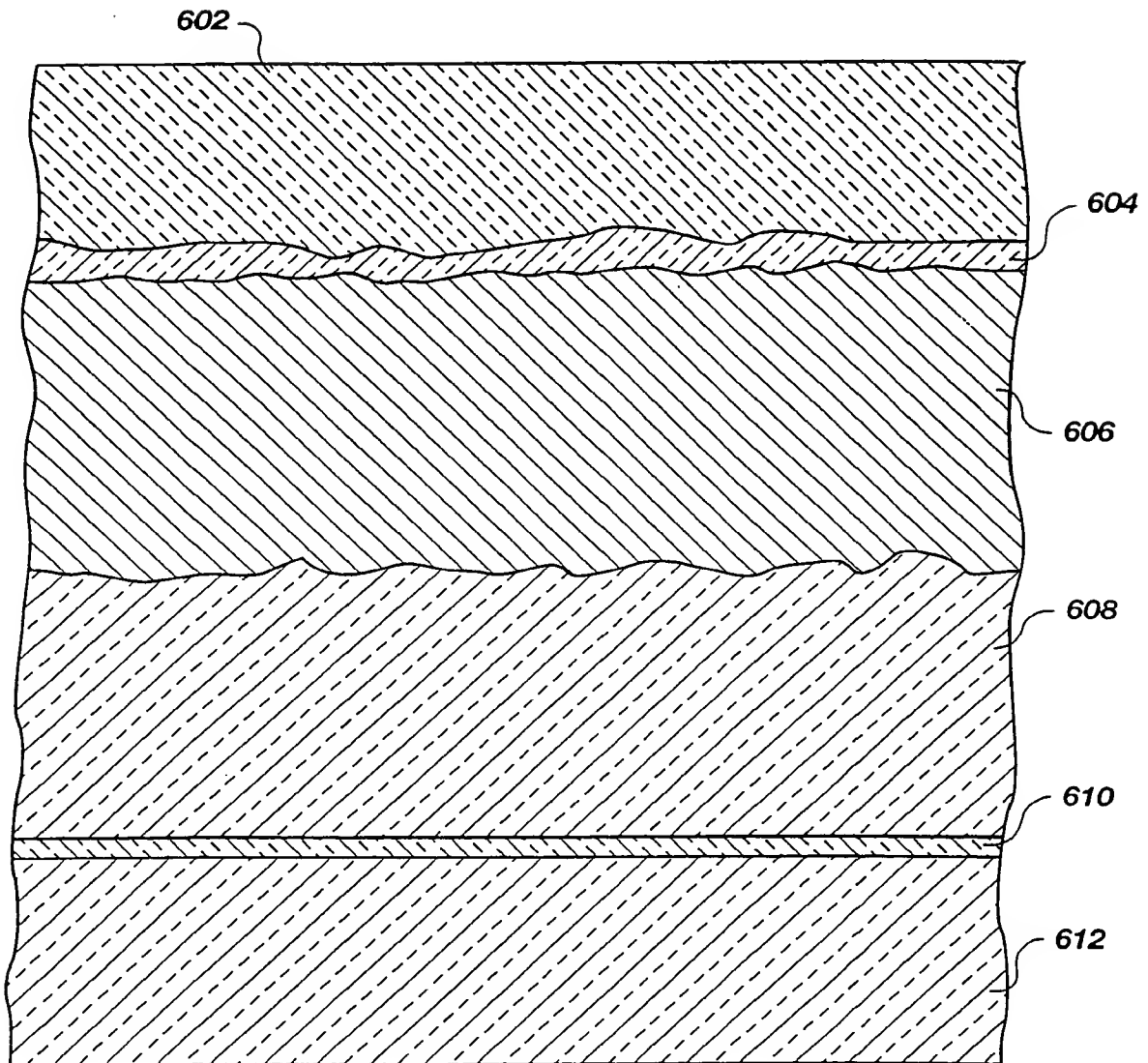


Fig. 24